IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kalvin E. Williams et al.		
Assignee:	LSI Logic Corporation		
Title:	METHOD FOR MULTIPROCESSOR COMMUNICATION WITHIN A SHARED MEMORY ARCHITECTURE		
Serial No.:	09/915,833	Filed:	July 26, 2001
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Attorney Docket No.:	1496.00136		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF KALVIN E. WILLIAMS PURSUANT TO 37 C.F.R. S 1.132

I, Kalvin E. Williams hereby declare as follows:

1. I am presently a Design Manager for LSI Logic Corporation and have been employed by LSI in various capacities for more than seven years. My Curriculum Vitae is attached as Appendix A.

2. I have reviewed the claims of the present invention. In particular, claim 1 of my invention provides:

> An apparatus comprising:
>
> a shared memory configured to store data; and

a multiprocessor logic circuit comprising (i) a plurality of processors and (ii) a message circuit, wherein (a) said message circuit is a configured to pass messages between said processors and (b) each of said processors is configured to access said shared memory through a system bus.

3. The distributed memory shown in FIG. 3 of Yamada (elements 21-1, 21-2 and 21-3) does not appear to be accessible through the so-called system bus (the processor interconnect 25).

4. The processor 19-1 accesses the memory 21-1 through the processor bus 30-1, not the so-called system bus 25.

5. The processor 19-2 accesses the memory 21-2 through the processor bus 30-2, not the so-called system bus 25.

6. Yamada clearly states in column 6, lines 57-59 that "the processor 19-1 is able to access the distributed shared memory (DSM) 21-1, but is unable to access the other DS memories 21-2 and 21-3".

7. Yamada, by its own explanation, presents a series of distributed memories that are not the same as the claimed shared memory configured to be accessed by **each** of a plurality of processors.

8. The various distributed memories of Yamada are not accessible as in the presently claimed invention.

9. If the distributed memories 21-1, 21-2 and 21-3 are considered to be a single memory (as asserted in the Office Action), then **each** of the processors 19-1, 19-2 and 19-3 are not able to access the distributed memory of Yamada.

10. The processor 19-1 is unable to access the distributed memories 21-2 and 21-3.

11. While Aschmann may show a memory, Aschmann, alone or in combination with Yamada, do not disclose or suggest a memory and message circuit configured to pass messages between the processors.

12. I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or patents issued therefrom.

Date: 21st January 2005

Kalvin E. Williams

APPENDIX A

CURRICULUM VITAE

NAME: Kalvin E. Williams

ADDRESS: 16 Celandine Grove
Thatcham, Berkshire
England RG18 4EE

EDUCATION

9/1989-7/1992 Staffordshire University
Electrical Engineering - 2.i BEng Hons

PROFESSIONAL QUALIFICATIONS

EMPLOYMENT HISTORY

1. **LSI Logic Europe Ltd**

Greenwood House,
London Road, Bracknell

A design centre for LSI Logic Corporation. Designers of Audio, Video Decoder and Encoder VLSI semiconductor devices for Digital Television (DTV) and Digital Versatile Disk (DVD) products.

6/2004- Present - **Design Manager**
Leading a group of four (including myself), I am responsible for subsystem design and delivery for LSI Logic's latest DVD Recorder Encoder/Decoder devices. Typically, this involves assessing the work required for a given development and generating a corresponding functional specification. I provide timescale estimates for the project and generate a committed project plan. The plan spans; resolving open issues, design, development, verification and delivery to a chip integration team. During the development, I am responsible for tracking the project and keeping to schedule. I provide

technical guidance to the engineers implementing the design, resolving issues as they arise and liasing with other departments/engineers as necessary.

8/2000-5/2004 - **Staff Engineer**
Systems Architect within the Decoder Design group. Initially, this involved working on Set Top Box decoder devices, but later my product focus switched to encoder/decoder devices for DVD Recorders. The role involved reviewing external (market driven) specifications, assessing product requirements and evaluating the design implications. I would meet with customers, reviewing their specific applications to identify areas for improvement within our product in order to reduce our customers' future system costs. I would generate functional specifications for modules to be developed and then work closely with various design teams to ensure the designs were fit for purpose and operating as required by these specifications. I was responsible for developing a products infrastructure and modeling the system to ensure the design met performance targets prior to committing to the detailed design. The promotion to Staff Engineer was a move along the Technical Expert career path within LSI Logic. This grade is considered to be level with that of a Manager and has exacting requirements within the company. In addition to generating device architectures, I personally implemented the design, development and test of some sub modules and the management of subcontractors implementing the design, development and test of others.

1/2000-7/2000 - **Principal Engineer**

1/1999-12/1999 - **Principal Engineer**
Hardware Design Engineer and Technical Lead within the Bracknell based Set Top Box (STB) System Applications group. The role involved the design and development of device verifications platforms (for LSI internal use), evaluation systems (for LSI demonstrations and customer evaluation), custom reference designs and customer circuit review. The verification platforms consisted of relatively large and complex PCB's capable of running the target DTV devices across their full range of functionality. Further, the design extended beyond the scope of a conventional STB by including high specification FPGA devices for real time data acquisition and logging. In the event of a device issue, the role of the FPGAs would be to capture datasets which would help reveal the source of the issue. The verification platform would also be the first platform used when a new chip design was returned from fabrication and initially powered. Evaluation platforms were a demonstration of the common functions of the chip. Hence, the design would be slightly more complex than most commercial STBs but significantly less complex than the verification platforms. Reference designs would be fully featured STBs, designed to a customers specification. The design would then be manufactured by the customer themselves. If desired, a customers circuit could also be reviewed within the group and feedback provided. This was a facility usually reserved for early access partners. The role also required some post silicon verification and the provision of technical support to our Field Application Engineers. Finally, the role involved investigating new applications and detailing how existing products could be designed into said applications.

5/1998-12/1998 - **Senior Engineer**

2. **Pioneer Digital Design Centre Ltd (Division of Pioneer GB Ltd)**
Almondsbury Business Park,
Almondsbury, Bristol

A development centre within the corporate Research and Development division of Pioneer.

6/1997-4/1998 - **Senior Hardware Engineer**
Sole hardware engineer within the group, I was responsible for developing a cost sensitive DVB compatible digital Set Top Box reference design for the OnDigital competitive bid returns (the original Digital Terrestrial TV service launched within the UK). Tasks involved review of EMC and BABT standards, investigation, evaluation and selection of various chip set solutions, analogue and digital circuit design, schematic capture and liasing with contract PCB layout designers.

3. **Pentica Systems Ltd, Oaklands Park Industrial Estate**
Wokingham, Berkshire

Designers, manufacturers and distributors of In Circuit Emulators (ICE). Product specialist for 8 and 16 bit Motorola processors – Motorola's emulator manufacturer of choice for in house developments (pagers etc.).

6/1997-4/1998 - **Senior Hardware Engineer**
Designated the product owner of the Mime 600 range of In Circuit Emulators, I was responsible for the development of new emulator variants for emerging micro controllers and providing technical support to the in house service department. Designs were often started whilst the target micro controller was still in development. Hence, initial work would be based on both early revisions of device specification and direct communication with the chip designers prior to prototype parts being available. Designs typically consisted of an Emulator Pod which carried the target micro controller and a main unit containing program memory connected via approximately 0.5m of ribbon cabling. Various stages of multiplexing and signal routing existed to facilitate switching between monitor and application program memory banks. This enforced environment, typically considered electrically poor, mandated designs which were carefully considered in terms of signal timing, signal integrity and electromagnetic compatibility. Being a small company, my duties spanned analogue and digital circuit design, schematic entry, PCB layout, FGPA code development, software development and production of manufacturing documentation. I developed emulator variants for Motorola's 68HC05 and 68HC11 micro controllers, Ford's custom microprocessor (Epic) for automotive engine management systems and Toshiba's TLCS900 series of microprocessor.

4. **Digi-Media Vision Ltd (Initially the Advanced Products Division of NTL, subsequently a Division of News Digital Systems)**
Crawley Court, Crawley

Design centre for Digital Television Broadcast equipment (Encoders, Decoders and Multiplexers) and reference designs for consumer products.

8/1995-2/1996 - **Development Engineer**
Located within the Consumer Set Top Box (STB) group, I was exclusively responsible for maintaining the reference hardware designs for DVB (Digital Video Broadcasting) based MPEG2 STBs. Duties involved updating schematics to incorporate the latest in house design of Transport Stream Demultiplexor, third party audio & video decoder and video standards encoder (PAL, NTSC etc.). Further duties involved maintaining third party product matrix's summarizing alternate chipset solutions and the definition of a Hardware Driver Interface (HDI) for use within commercial STBs.

5. **Lucas Body Systems (Division of Lucas Automotive Electronics Ltd)**
Windrush Industrial Park,
Witney, Oxfordshire

Design centre for Automotive Body Electronics – Alarm systems, Trip Computers, Display Units, Central Door Locking controllers, Multi-function "Black Box" Controllers, Remote Entry Keys, Engine Immobilisers etc.

5/1995-8/1995 - **Senior Design Engineer**
Working within the SAAB customer team (total of 3 engineers and 1 manager), I was responsible for the design of Hardware and Real Time Embedded Software for Secondary Displays, Body Control Units and Alarm Systems within the SAAB 900 and SAAB 95 range of vehicles. Duties spanned: initial concept development; detailed product design; direction of PCB layout engineers; Prototype and Production Build documentation; product testing (against functional specifications, environmental conditions, Electro Magnetic Compatibility / Susceptibility and Electrostatic Discharge Immunity) and liaison with production facilities to ensure the product design was suitable for high volume manufacture. Designs were typically mixed signal. Analogue circuitry would be for bulb circuit sensing, FET gate drive voltage doubling via charge pumps for high side FET based switching or ambient light sensing circuits for display backlight driving. Digital circuits typically involved an 8 bit 68HC05 series of micro controller with additional multiplexing for digital inputs and signal switching for outputs. Software was developed with a structured design methodology (Yourdon). Failure Mode Event Analysis would also be undertaken to evaluate design risks. I also undertook: technical assessments and costing of competitor products; initial design and cost estimates for competitive bid returns and the development of demonstrator products which included the supervision of their installation within vehicles. I also undertook updates to existing products and review of manufacturing line process's to improve production yields.

9/1993-5/1995 - **Design Engineer**

6. **AEA Technology (United Kingdom Atomic Energy Authority)**
Harwell Laboratory
Didcot, Oxfordshire

7/1992-9/1993 - **Building Controls Engineer**
On returning to full time work after University, I was assigned to the Site Services Division of Harwell and Culham (near Abingdon) Laboratories. I was responsible for maintaining the "Trend" Intelligent Building Management systems used on both sites and the project management of building renovations from legacy heating controls to the new intelligent system. I was also responsible for health and safety issues arising within site plant rooms. This involved regularly inspecting plant rooms for faults/issues and maintaining records for stored substances (COSHH assessments).

9/1989-7/1992-
Three years unpaid leave to attend Staffordshire University (to study my degree in Electronic Engineering). I returned to work during all major vacation periods as an Electronic Instrument Mechanic.

9/1985-9/1989 - **Apprentice Electronic Instrument Mechanic**
Four year Skilled Craft apprenticeship for Atomic Energy Authority prior to University. The first two years were spent within the training school. Of this, the first 6 months covered mechanical appreciation which included sheet metal work, turning & milling. The subsequent 6 months covered electrical skills; soldering techniques, wiring (ring mains, lighting circuits and 3 phase motor starters) and installation. The second year taught electronic design, assembly and fault finding. The final two years were spent "on site", generally with 3 month placements in various departments. Experience during this time covered: circuit fault finding and repair; plant installation; instrument calibration; circuit assembly and design. Throughout the four years, Newbury College was attended on a part time basis to study both an ONC and HNC in Electronics.

APPENDIX A

PUBLICATIONS

United States Patent No. 6,795,874 B2, Issued 9/2004, Entitled: Direct Memory Accessing